REMARKS

Claims 1-20 were pending in this application.

Claims 1-20 have been rejected.

Claims 1, 3, 6, 9, 10, and 13 have been amended as shown above.

Claims 1-20 remain pending in this application.

Reconsideration and full allowance of Claims 1-20 are respectfully requested.

I. AMENDMENTS TO SPECIFICATION

The Office Action requests that the Applicants provide the serial numbers for ten related patent applications. The Applicants have amended the "Cross-Reference to Related Applications" section to include the serial numbers for the related patent applications.

II. REJECTION UNDER 35 U.S.C. § 102

The Office Action rejects Claims 15-18 under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,282,633 to Killian ("*Killian*"). The Applicants respectfully traverse this rejection.

A prior art reference anticipates the claimed invention under 35 U.S.C. § 102 only if every element of a claimed invention is identically shown in that single reference, arranged as they are in the claims. (*MPEP § 2131; In re Bond, 910 F.2d 831, 832, 15 U.S.P.Q.2d 1566, 1567 (Fed. Cir. 1990)*). Anticipation is only shown where each and every limitation of the claimed invention is found in a single prior art reference. (*MPEP § 2131; In re Donohue, 766 F.2d 531,*

534, 226 U.S.P.Q. 619, 621 (Fed. Cir. 1985)).

Killian recites a RISC processor implementing an instruction set that has a smaller number of instructions for programs and a smaller average number of bits per instruction. (*Abstract*). Among other things, the processor includes a decoder (element 201), a multiplexer (element 432), and a load align circuit (element 436). (*Col. 7, Lines 20-28*). During a load instruction, the multiplexer provides either a data value from a cache or a data value from an external memory to the load align circuit. (*Col. 7, Lines 20-23*). The load align circuit then shifts and sign-extends the data value received from the multiplexer. (*Col. 7, Lines 23-28*).

Regarding Claim 15, this portion of *Killian* simply recites shifting and sign-extending data retrieved from a cache or from an external memory. This portion of *Killian* fails to disclose "receiving in a sign extender unit an input syllable that contains a K bit field containing K bits that represent a short constant operand" as recited in Claim 15. While the load align circuit of *Killian* receives a data value, the data value represents a value from a cache or an external memory. This portion of *Killian* contains absolutely no mention that the load align circuit is capable of receiving a "short constant operand" that is contained in an "input syllable" as recited in Claim 15. In fact, this portion of *Killian* contains no mention that the load align circuit receives any "input syllables" at all. This portion of *Killian* also contains absolutely no mention of using a "short constant operand" in any way. While a previous portion of *Killian* refers to decoding constants (column 5, lines 52-63), this portion of *Killian* is describing the operation of a decoder (element 201), not the load align unit. The Office Action fails to show that the decoder of *Killian* includes a "sign extender unit" that receives and right justifies K bits in a K

bit field of an input syllable.

Because of this, the Office Action fails to show that the load align unit or the decoder of *Killian* anticipates "receiving in a sign extender unit an input syllable that contains a K bit field containing K bits that represent a short constant operand" as recited in Claim 15. As a result, the Office Action fails to show that *Killian* anticipates all elements of Claim 15.

Regarding Claim 18, these portions of *Killian* simply recite that the load align unit performs shift and sign-extension functions and that the decoder can decode constants. These portions of *Killian* contain absolutely no mention of separately receiving an "extension syllable" that contains a "T bit field containing T bits that represent the high order bits of [a] long constant operand" and a "first instruction syllable" that contains "a K bit field containing K bits that represent the low order bits of said long constant operand" as recited in Claim 18. These portions of *Killian* also contain absolutely no mention of placing the separately received "T bit field" and "K bit field" on different data paths and combining the bits on a third data path so the "combination of said K bits and said T bits represent said long constant operand" as recited in Claim 18. The fact that *Killian* may mention the use of different lengths for operands does not anticipate the specific elements recited in Claim 18. As a result, the Office Action fails to show that *Killian* anticipates all elements of Claim 18.

For these reasons, the Office Action fails to show that *Killian* anticipates the Applicants' invention as recited in Claims 15 and 18 (and their dependent claims). Accordingly, the Applicants respectfully request withdrawal of the § 102 rejection and full allowance of Claims 15-18.

III. REJECTION UNDER 35 U.S.C. § 103

The Office Action rejects Claims 1-14 and 20 under 35 U.S.C. § 103(a) as being unpatentable over *Killian* in view of U.S. Patent No. 6,006,324 to Tran ("*Tran*"). The Office Action rejects Claim 19 under 35 U.S.C. § 103(a) as being unpatentable over *Killian*. The Applicants respectfully traverse these rejections.

In *ex parte* examination of patent applications, the Patent Office bears the burden of establishing a *prima facie* case of obviousness. (*MPEP § 2142; In re Fritch, 972 F.2d 1260, 1262, 23 U.S.P.Q.2d 1780, 1783 (Fed. Cir. 1992)*). The initial burden of establishing a *prima facie* basis to deny patentability to a claimed invention is always upon the Patent Office. (*MPEP § 2142; In re Oetiker, 977 F.2d 1443, 1445, 24 U.S.P.Q.2d 1443, 1444 (Fed. Cir. 1992); In re Piasecki, 745 F.2d 1468, 1472, 223 U.S.P.Q. 785, 788 (Fed. Cir. 1984)*). Only when a *prima facie* case of obviousness is established does the burden shift to the applicant to produce evidence of nonobviousness. (*MPEP § 2142; In re Oetiker, 977 F.2d 1443, 1445, 24 U.S.P.Q.2d 1443, 1444 (Fed. Cir. 1992); In re Rijckaert, 9 F.3d 1531, 1532, 28 U.S.P.Q.2d 1955, 1956 (Fed. Cir. 1993)*). If the Patent Office does not produce a *prima facie* case of unpatentability, then without more the applicant is entitled to grant of a patent. (*In re Oetiker, 977 F.2d 1443, 1445, 24 U.S.P.Q.2d 1443, 1444 (Fed. Cir. 1992); In re Grabiak, 769 F.2d 729, 733, 226 U.S.P.Q. 870, 873 (Fed. Cir. 1985)*).

A *prima facie* case of obviousness is established when the teachings of the prior art itself suggest the claimed subject matter to a person of ordinary skill in the art. (*In re Bell, 991 F.2d 781, 783, 26 U.S.P.Q.2d 1529, 1531 (Fed. Cir. 1993)*). To establish a *prima facie* case of

obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed invention and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. (*MPEP § 2142*).

Regarding Claim 1, as described above in Section II, *Killian* contains no mention of receiving "at least one syllable" and then "right justifying ... K bits" to produce a "short constant operand" or combining "K bits" with "T bits" to produce a "long constant operand" as recited in Claim 1. As a result, the Office Action fails to show that *Killian* discloses, teaches, or suggests all elements of Claim 1.

Regarding Claims 19 and 20, Claims 19 and 20 depend from Claim 18. As shown above in Section II, Claim 18 is patentable. As a result, Claims 19 and 20 are patentable due to their dependence from an allowable base claim.

For these reasons, the Office Action fails to establish a *prima facie* case of obviousness against Claim 1 (and its dependent claims) and Claims 19 and 20. Accordingly, the Applicants respectfully request withdrawal of the § 103 rejections and full allowance of Claims 1-14, 19, and 20.

IV. CONCLUSION

As a result of the foregoing, the Applicants assert that all claims in this application are in condition for allowance and respectfully request an early allowance of such claims.

SUMMARY

If any issues arise, or if the Examiner has any suggestions for expediting allowance of this application, the Applicants respectfully invite the Examiner to contact the undersigned at the telephone number indicated below or at ***wmunck@davismunck.com***.

The Commissioner is hereby authorized to charge any additional fees connected with this communication (including any extension of time fees) or credit any overpayment to Deposit Account No. 50-0208.

Respectfully submitted,

DAVIS MUNCK, P.C.

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